IPC India

IPC India workshop, Hand Soldering competition and PCB design competition

The supporting program for productronica India 2019 will be finalized in summer 2019. In the meantime you may check the supporting program of productronica India 2018 below.

IPC India–the Indian office of global electronics standards organization IPC (US HQ) at electronica India and productronica India.

IPC Hand Soldering competition	
Date:	September 26–27, 2018
Venue:	Hall 3, BIEC, Bengaluru
Organized by:	IPC India

“Reliability of any electronic equipment is measured by a zero-defect soldering process”.

The task for the competing participants is to build a functional electronics assembly within a given time limit.

Competence of the assembly is judged by Master Trainers in accordance with IPC-A-610G Class 3 criteria, the speed at which the assembly is produced and also overall electrical functionality of the assembly. The IPC Hand Soldering competition will be held on September 26–27, 2018 and the result will be declared on September 27, 2018.

The preliminary contest winner gets a certificate along with FREE admission to IPC- J-STD-001 CIS training and certification course and the runner up

SAVE THE DATE

productronica India | International Trade Fair for Electronics Development and Production

Date: Sep 25 - 27, 2019

Your contact

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gets a certificate along with FREE admission to IPC-A-610 CIS training and certification course.

The first and the second place will be participating in the “IPC India national level competition” on September 28, 2018. The winner of the Indian championship will have a chance to participate in “World level hand soldering competition championship”, SAN DIEGO convention center, CA, USA

IPC India workshop	
Date:	September 27, 2018
Time:	09:30–13:00
Venue:	Hibiscus hall, Conference Center, BIEC, Bengaluru
Speaker:	Mr. S L N Murthy
Organized by:	IPC India

The emergence of technologies and smaller device features has given rise to new silicon families. More devices are packed under each package and power demands are on the rise. The thrust to pack more data in each data stream has moved the data transfer from parallel to serial mode of data transfer. These have faster switching rates. Thus, every design in a system is turning out to be falling into the multi-gigahertz domain.

Designing interconnects from end to end and validating them for performance is gaining more momentum. At higher data rates, the dielectric material contributes to high signal losses and the skin effect, surface finish requires a review based on the same. In this short overview, we look at the various challenges that must be taken cognizance of during the PCB design engineering flow. The challenges in power delivery network design to ensure that operating needs of the devices are addressed.

The objective of this program is to understand the parameters that influence signal integrity and power integrity of the PCB design flow. Without dwelling into the mathematical aspects, underlining principles, solution space analysis and final assertion of design functionality is presented.

IPC India workshop (636 kB PDF-document)

IPC India PCB design competition	
Date:	September 27, 2018
Time:	14:30–17:30
Venue:	Hibiscus hall, Conference Center, BIEC, Bengaluru
Organized by:	IPC India

The IPC India PCB design competition 2018 will focus on testing the skills of the PCB designers and create opportunities to compete with the best in the business.

For further information please check the official website of IPC India

↗ IPC India PCB design competition

Organizer

IPC India